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(54) Title: COMPOSITE PRINTING

(57) Abstract: Systems and techniques for printing substrates. In one implementation, a method includes patterning a substrate with a substantially arbitrary arrangement of features by introducing irregularity into a repeating array of features.

COMPOSITE PRINTING

BACKGROUND

This disclosure relates to the printing of substrates.

Various lithographic techniques can be used to print
5 patterns such as those that define integrated circuits in
microelectronic devices. For example, optical lithography,
e-beam lithography, UV and EUV lithography, x-ray
lithography and imprint printing techniques can all be used
to form micron- and submicron-sized features.

10

DESCRIPTION OF DRAWINGS

FIG. 1 is a top view of a wafer.

FIG. 2 is a sectional view of a portion of a layout
piece on a wafer during processing.

FIG. 3 is a top view of a layout piece after exposure
15 and development to form a two-dimensional array of features.

FIG. 4 is a sectional view of the layout piece of FIG.
3.

FIGS. 5, 6, and 7 are sectional views along the same
plane as FIG. 4 after additional processing.

20 FIG. 8 shows a top view of a layout piece after
exposure and development to form a pattern.

FIG. 9 shows a sectional view of the layout piece of
FIG. 8.

FIGS. 10 and 11 are sectional views along the same plane as FIG. 9 after additional processing.

FIG. 12 shows a top view of a layout piece after removal of a sacrificial layer.

5 FIG. 13 shows a sectional view of the layout piece of FIG. 12.

FIG. 14 shows a composite optical lithography system.

FIG. 15 shows an example patterning system in the composite optical lithography system of FIG. 14.

10 Like reference symbols in the various drawings indicate like elements.

DETAILED DESCRIPTION

FIG. 1 shows a top view of a wafer 100. Wafer 100 is a semiconductor wafer being processed to form at least one integrated circuit device such as a microprocessor, a chip set device, or a memory device. For example, wafer 100 can be used to form a collection of SRAM memory devices. Wafer 100 can include silicon, gallium arsenide, or indium phosphide. Wafer 100 includes an array of die portions 105. 15 Wafer 100 can be diced or otherwise processed to form a collection of dice that can be packaged to form individual integrated circuit devices. Each die portion 105 includes one or more layout pieces 110. A layout piece 110 is a section of a die portion 105 that includes a pattern. The 20

pattern defined in a layout piece 110 generally contributes to the function of integrated circuit devices formed from die portions 105.

FIG. 2 is a sectional view of a portion of layout piece 110 on wafer 100. At the processing stage illustrated in FIG. 2, layout piece 110 includes a substrate 205, a pattern layer 210, a sacrificial layer 215, and a printing layer 220. Substrate 205 can be the base wafer or another layer formed during previous processing. Pattern layer 210 is the portion of layout piece 110 that is to be patterned. Pattern layer 210 can be patterned to form all or a portion of a microelectronic device. Pattern layer 210 can be, e.g., an electrical insulator such as silicon dioxide or nitride, a semiconducting material such as p- or n-doped silicon, or a conducting layer such as copper or aluminum. Sacrificial layer 215 is a temporary layer that can be selectively removed from pattern layer 210. Sacrificial layer 215 can be an interlayer dielectric (ILD) such as a silicon oxide or nitride. Printing layer 220 is a material that is sensitive to one or more techniques for printing patterns. For example, printing layer 220 can be a positive or negative photoresist. The following description assumes printing layer 220 to be a positive photoresist.

Resist layer 220 can be exposed and developed to form a pattern. FIG. 3 is a top view and FIG. 4 is a sectional

view of layout piece 110 after exposure and development to form a two-dimensional array 300 of repeating features 305. Features 305 repeat in array 300 in that, excepting manufacturing defects and other irregularities in individual features 305, array 300 includes a repetitive order or arrangement of individual features 305. Array 300 can be rectangular or square with a length 310 and a width 315 that occupies all or a portion of layout piece 110. Features 305 in array 300 have a pitch 320. The pitch of features is the smallest spatial periodicity of the features. For example, contact pitch 320 is the sum of the width 325 of a contact 305 and the shortest distance 330 to the next nearest contact 305. Only a single pair of contacts 305 need be at pitch 320. Thus, the separation distance and width of contacts 305 can vary (e.g., in the horizontal and vertical directions) and array 300 can still have pitch 320.

Features 305 can be formed using any of a number of different lithographic techniques such as e-beam lithography, interference lithography, and optical lithography using phase-shifting masks and optical proximity correction techniques. These lithographic techniques can involve the exposure of wafer 100 using an interference pattern. For example, features 305 can be formed using interference lithography by exposing resist 220 using two orthogonal sets of interfering laser beams with a wavelength

λ_1 to form the array of features with pitch 320 approaching $\frac{1}{2}\lambda_1$. The orthogonal sets can be generated by splitting a single source four ways using a pyramidal prism and interfering the reflections from two orthogonal pairs of opposing pairs of mirrors. The orthogonal pairs can illuminate a substrate at different angles of illumination or the orthogonal pairs can illuminate a substrate at the same angle of illumination. Illuminating at the same angle can impart the substrate with the same pitch in both, 5 orthogonal, directions. Alternatively, the orthogonal sets can be generated by double exposing resist 220 after wafer 100 is subject to a 90° rotation in a traditional interferometric lithography system.

Features 305 can display features characteristic of the 15 lithographic technique used to form features 305. For example, when features 305 are formed using interference lithography, features 305 can be formed with a definition characteristic of interference lithography and a pitch approaching $\frac{1}{2}\lambda_1$ with minimal feature distortion of the type 20 that arises due to imperfections in projection printing systems and techniques. For example, features 305 can be formed without imperfections that arise due to the use of a mask, lenses, projection optics, and/or the backscattering of electrons. Features 305 can also show the influence of

the relatively large depth of focus provided by interferometric lithography techniques. For example, the relatively large depth of focus can provide precise control of the dimensional characteristics of features, especially 5 relative to the control provided by optical systems in which high numerical apertures limit both the depth of field and the ability to print real world substrates that are not ideally flat.

FIGS. 5, 6, and 7 are sectional views along the same 10 plane as FIG. 4 after additional processing. In particular, FIG. 5 shows layout piece 110 after an etch has defined cavities 505 in sacrificial layer 215. For example, cavities 505 can be defined using a dry plasma etch. Cavities 505 can inherit the character of features 305 that 15 are characteristic of the lithographic technique used to form features 305. For example, when features 305 are exposed using interference lithography, cavities 505 can inherit the definition characteristic of interference lithography where minimal pitch approaches $\frac{1}{2}\lambda_1$ with minimal 20 feature distortion of the type that arises due to imperfections in projection printing systems and techniques. Cavities 505 can be generally cylindrical with their axes oriented perpendicular to the plane of wafer 100. Cavities 505 can be defined to have substantially the same pitch 320 25 as features 305. Cavities 505 can have diameters smaller,

larger, or substantially the same as the diameters of features 305, depending on the etch process selected to define cavities 505.

FIG. 6 shows layout piece 110 after resist 220 has been
5 stripped. FIG. 7 shows layout piece 110 after a new resist layer 705 has been formed above sacrificial layer 215.

Resist layer 705 can either cap or fill cavities 505 of sacrificial layer 215. Resist layer 705 can be formed, e.g., by spin coating photoresist on wafer 100.

10 FIG. 8 shows a top view and FIG. 9 shows a sectional view of layout piece 110 after resist layer 705 has been exposed and developed to form a figure 805. Figure 805 can be arbitrarily shaped in that figure 805 need not include a repetitive order or arrangement. Figure 805 is aligned with
15 the two-dimensional array of cavities 505 to either expose (for example, at 810) or cover (for example, at 815) individual cavities 505.

Figure 805 can be formed with a length 820 and a width

825 that occupies all or a portion of layout piece 110.

20 Figure 805 can include elements with a pitch 830. Pattern element pitch 830 is the sum of the width 835 of an element 840 and the shortest distance 845 to the next nearest element 850. Only a single pair of elements in figure 805 need be at pitch 830. Thus, the separation distance and
25 width of elements can vary, and figure 805 can still have

pitch 830. Pitch 830 can be two or more times as large as contact pitch 320.

Since pattern pitch 830 can be relatively larger than contact pitch 320, figure 805 can be formed using

5 lithographic systems and techniques that have a lower resolution than the systems and techniques used to form features 305. For example, if features 305 are formed using an interferometric lithography system with a wavelength λ_1 , then figure 805 can be formed using an optical lithography system with a wavelength larger than λ_1 . As another example, 10 figure 805 can be formed using a traditional binary optical lithography system, or other lithographic systems such as imprint and e-beam lithographic systems capable of achieving the lower resolution.

15 The exposure or shielding of cavities 505 by figure 805 can be used to introduce irregularity into the repeating array of cavities 505 after hardening of resist 705. In other words, the arbitrary shape of figure 805 can be used to stop the periodic reoccurrence of features in layout 20 piece 110.

FIGS. 10 and 11 are sectional views along the same plane as FIG. 8 after additional processing. In particular, FIG. 10 shows layout piece 110 after an etch has defined cavities 1005 in pattern layer 210. For example, cavities 25 1005 can be defined using a dry plasma etch. Cavities 1005

can inherit, by way of cavities 505, the character of features 305 that are characteristic of the lithographic technique used to form features 305. For example, when features 305 are exposed using interference lithography, 5 cavities 1005 can inherit, by way of cavities 505, the definition characteristic of interference lithography with minimal feature distortion of the type that arises due to imperfections in projection printing systems and techniques at a pitch approaching λ_1 . Cavities 1005 can be generally 10 cylindrical, with their axes oriented perpendicular to the plane of wafer 100. Cavities 1005 can be defined to have substantially the same pitch 320 as features 305. Cavities 1005 can have diameters smaller, larger, or substantially the same as the diameters of cavities 505.

15 FIG. 11 shows layout piece 110 after resist 705 has been stripped to expose previously covered cavities 505. FIGS. 12 shows a top view and FIG. 13 shows a sectional view of layout piece 110 after sacrificial layer 215 has been removed. Sacrificial layer 215 can be removed by chemical 20 mechanical polishing (CMP) or by etching. After removal of sacrificial layer 215 and the exposure of cavities 1005, pattern layer 210 in layout piece 110 includes a collection of pattern features 1205. Pattern features 1205 can be used in a functional design layout of a microelectronic device. 25 Pattern features 1205 can have pitch 320 that is limited by

the pitch available from the lithographic technique used to form contacts 305. Moreover, depending upon the geometry of resist figure 805, pattern features 1205 can also have an arbitrary arrangement in pattern layer 210 since, after 5 irregularity is introduced into repeating array 300, the impact of at least some of the small pitch features 305 upon wafer 100 has been eliminated.

Such composite patterning can prove advantageous. For example, a single layout piece can be patterned with 10 features using a higher resolution system or technique and the functional impact of those features can be modified or even eliminated using a lower resolution system or technique. For example, older, typically lower resolution, equipment can be used to modify the impact of higher 15 resolution features, providing increased lifespans to the older equipment. Patterning cost can be decreased by devoting high resolution systems to the production of high resolution features while using less expensive, lower resolution systems for the modification of the impact of 20 those high resolution features. For example, high resolution but relatively inexpensive interferometric systems can be combined with relatively inexpensive low resolution systems to produce high quality, high resolution patterns without large capital investments. Since the 25 arrangement of patterns produced using interferometric

systems can be changed using lower resolution systems, the applicability of interferometric systems can be increased. In particular, interferometric systems can be used to form substantially arbitrary arrangements of features that are 5 not constrained by the geometries and arrangements of interference patterns.

FIG. 14 shows a composite optical lithography system 1400. System 1400 includes an environmental enclosure 1405. Enclosure 1405 can be a clean room or other location 10 suitable for printing features on substrates. Enclosure 1405 can also be a dedicated environmental system to be placed inside a clean room to provide both environmental stability and protection against airborne particles and other causes of printing defects.

15 Enclosure 1405 encloses an interference lithography system 1410 and a patterning system 1415. Interference lithography system 1410 includes a collimated electromagnetic radiation source 1420 and interference optics 1425 that together provide interferometric patterning 20 of substrates. Patterning system 1415 can use any of a number of different approaches for patterning a substrate. For example, patterning system 1415 can be an e-beam projection system, an imprint printing system, or an optical projection lithography system. Patterning system 1415 can 25 also be a maskless module, such as an electron beam direct

write module, an ion beam direct write module, or an optical direct write module.

Systems 1410, 1415 can share a common mask handling subsystem 1430, a common wafer handling subsystem 1435, a 5 common control subsystem 1440, and a common stage 1445.

Mask handling subsystem 1430 is a device for positioning a mask in system 1400. Wafer handling subsystem 1435 is a device for positioning a wafer in system 1400. Control subsystem 1440 is a device for regulating one or more 10 properties or devices of system 1400 over time. For example, control subsystem 1440 can regulate the position or operation of a device in system 1400 or the temperature or other environmental qualities within environmental enclosure 1405.

15 Control subsystem 1440 can also translate stage 1445 between a first position 1450 and a second position 1455. Stage 1445 includes a chuck 1460 for gripping a wafer. At first position 1450, stage 1445 and chuck 1460 can present a gripped wafer to patterning system 1415 for patterning. At 20 second position 1455, stage 1445 and chuck 1460 can present a gripped wafer to interference lithography system 1410 for interferometric patterning.

To ensure the proper positioning of a wafer by chuck 1460 and stage 1445, control subsystem 1440 includes an 25 alignment sensor 1465. Alignment sensor 1465 can transduce

and control the position of the wafer (e.g., using wafer alignment marks) to align a pattern formed using interference lithography system 1410 with a pattern formed by patterning system 1415. Such positioning can be used 5 when introducing irregularity into a repeating array of features, as discussed above.

FIG. 15 shows an example optical lithographic implementation of patterning system 1415. In particular, patterning system 1415 can be a step-and-repeat projection 10 system. Such a patterning system 1415 can include an illuminator 1505, a mask stage 1510, and projection optics 1515. Illuminator 1505 can include an electromagnetic radiation source 1520 and an aperture/condenser 1525. Source 1520 can be the same as source 1420 or source 1520 15 can be an entirely different device. Source 1520 can emit at the same or at a different wavelength as source 1420. Aperture/condenser 1525 can include one or more devices for collecting, collimating, filtering, and focusing the 20 electromagnetic emission from source 1420 to increase the uniformity of illumination upon mask stage 1510.

Mask stage 1510 can support a mask 1530 in the illumination path. Projection optics 1515 can be a device for reducing image size. Projection optics 1515 can include a filtering projection lens. As stage 1445 repeatedly 25 translates a gripped wafer for exposure by illuminator 1505

through mask stage 1510 and projection optics 1515, alignment sensor 1465 can ensure that the exposures are aligned with a repeating array of interferometric features to introduce irregularity into the repeating array.

5 A number of implementations have been described.

Nevertheless, it will be understood that various modifications may be made. For example, both positive and negative resists can be used for either of resist layers 220, 705. Lithographic techniques that use different 10 wavelengths can be used to process the same substrate. Substrates other than semiconductor wafers can be patterned. Accordingly, other implementations are within the scope of the following claims.

WHAT IS CLAIMED IS:

1. A method comprising:

patterning a substrate with a substantially arbitrary arrangement of features by introducing irregularity into
5 a repeating array of features.

2. The method of claim 1, wherein introducing irregularity comprises forming an arbitrary figure above some of the features in the repeating array.

- 10 3. The method of claim 2, wherein patterning the substrate further comprises etching a substrate through portions of the repeating array not covered by the arbitrary figure.

- 15 4. The method of claim 1, wherein introducing irregularity comprises introducing irregularity into the repetition of features resulting from an interference pattern.

5. The method of claim 4, wherein introducing irregularity comprises introducing irregularity into the repetition of the interference pattern formed by interference lithography.

- 20 6. The method of claim 4, wherein introducing irregularity comprises introducing irregularity into the repetition

of the interference pattern formed by projection lithography.

7. The method of claim 1, wherein introducing irregularity comprises introducing irregularity into the repetition 5 of a two-dimensional array of contacts.

8. The method of claim 1, wherein patterning the substrate further comprises etching the substrate using the substantially arbitrary arrangement to direct the etching.

10 9. The method of claim 1, wherein patterning the substrate further comprises patterning the substrate with the substantially arbitrary arrangement having a pitch approaching one half the wavelength of a patterning electromagnetic radiation.

15 10. A device, comprising:

a substantially arbitrary arrangement of features, the features defined with a definition characteristic of interference lithography.

11. The device of claim 10, wherein the substantially 20 arbitrary arrangement of features comprises features printed with a pitch approaching one half the wavelength of a patterning electromagnetic radiation.

12. The device of claim 10, wherein the substantially arbitrary arrangement of features comprises features free from defects arising due to one or more of lens imperfections and mask imperfections.
- 5 13. The device of claim 10, wherein the substantially arbitrary arrangement of features comprises features free from defects arising due to backscatter of electrons.
- 10 14. The device of claim 10, wherein the substantially arbitrary arrangement of features comprises a portion of a microelectronic device.
15. The device of claim 14, wherein the portion of the microelectronic device comprises a portion of an SRAM memory device.
- 15 16. A system comprising:
 - a data processor;
 - an SRAM in data communication with the data processor, the SRAM including a substantially arbitrary arrangement of features, the features including definition characteristic of interference lithography.
- 20 17. The system of claim 16, wherein the SRAM comprises a substantially arbitrary arrangement of contacts

including definition characteristic of interference lithography.

18. A method comprising:

interfering electromagnetic radiation to illuminate a substrate with an interference pattern, the interference pattern imparting the substrate with repeating first features; and

introducing irregularity into the repetition of the interference pattern to impart a substantially arbitrary feature arrangement to the substrate.

19. The method of claim 18, wherein introducing irregularity comprises forming a substantially arbitrary figure above some portion of the interference pattern.

20. The method of claim 19, further comprises patterning the substrate using the substantially arbitrary figure to define the substantially arbitrary feature arrangement.

21. The method of claim 18, wherein interfering electromagnetic radiation comprises imparting, to the substrate, first features having a pitch approaching one half the wavelength of a patterning electromagnetic radiation.

22. The method of claim 18, wherein interfering electromagnetic radiation comprises using interference

lithography to illuminate the substrate with the interference pattern.

23. A method comprising:

patterning a substrate using a first lithographic technique, the patterning providing first features with a first pitch approaching one half the wavelength of a patterning electromagnetic radiation; and eliminating the impact of at least some of the first features on the substrate using a second lithographic technique providing second features with a second pitch, the second pitch being two or more times larger than the first pitch.

24. The method of claim 23, wherein patterning the substrate using the first lithographic technique comprises patterning the substrate using interference lithography.

25. The method of claim 24, wherein patterning the substrate using interference lithography comprises exposing the substrate with a pair of interference patterns.

26. The method of claim 25, wherein exposing the substrate comprises exposing the substrate with a substantially identical pair of interference patterns.

27. The method of claim 25, wherein exposing the substrate comprises exposing the substrate with the pair of interference patterns simultaneously.
28. The method of claim 23, wherein eliminating the impact of at least some of the first features on the substrate 5 comprises patterning using a binary mask.
29. The method of claim 23, wherein eliminating the impact of at least some of the first features on the substrate comprises printing an arbitrary figure above some of the 10 first features.
30. The method of claim 29, wherein eliminating the impact of at least some of the first features on the substrate further comprises etching a portion of the substrate through the first features not covered by the arbitrary 15 figure.
31. An apparatus comprising:
an interference exposure module to produce a first exposure resulting in an array of repeating contacts in a photosensitive media; and
20 a second patterning module to reduce regularity of the features in the array.
32. The apparatus of claim 31, wherein the interference exposure module comprises:

a pyramidal beam splitter to split an electromagnetic radiation four ways; and

two sets of opposing pairs of mirrors disposed to create an interference pattern by reflecting the split electromagnetic radiation.

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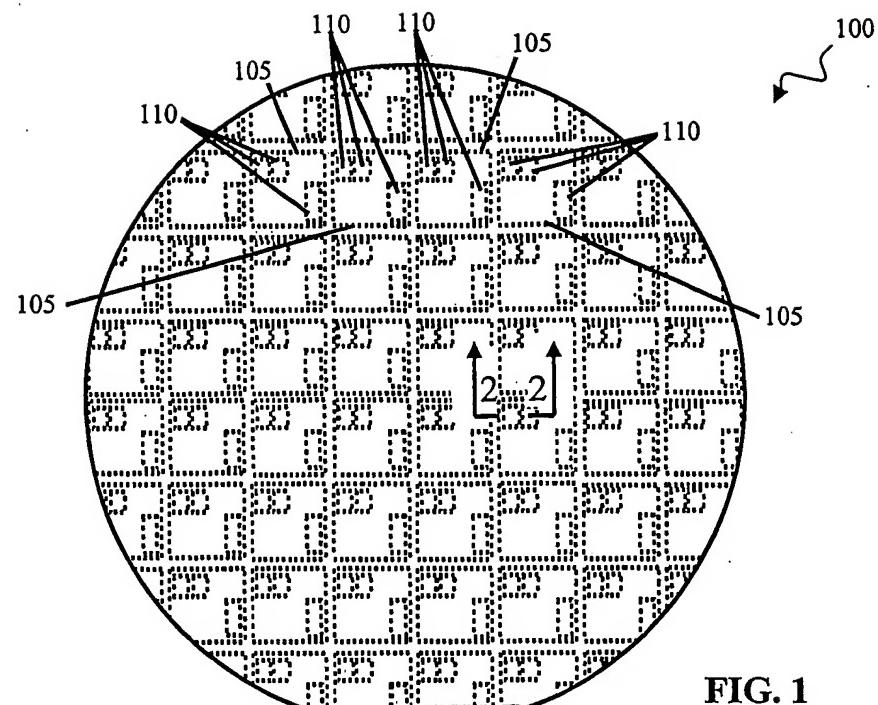


FIG. 1

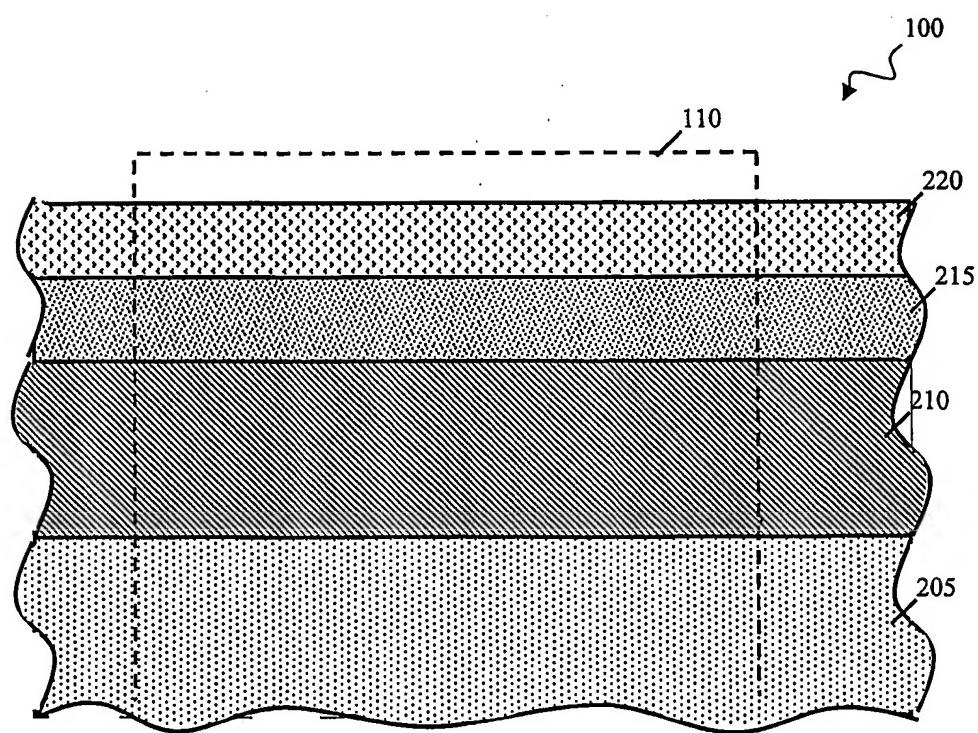


FIG. 2

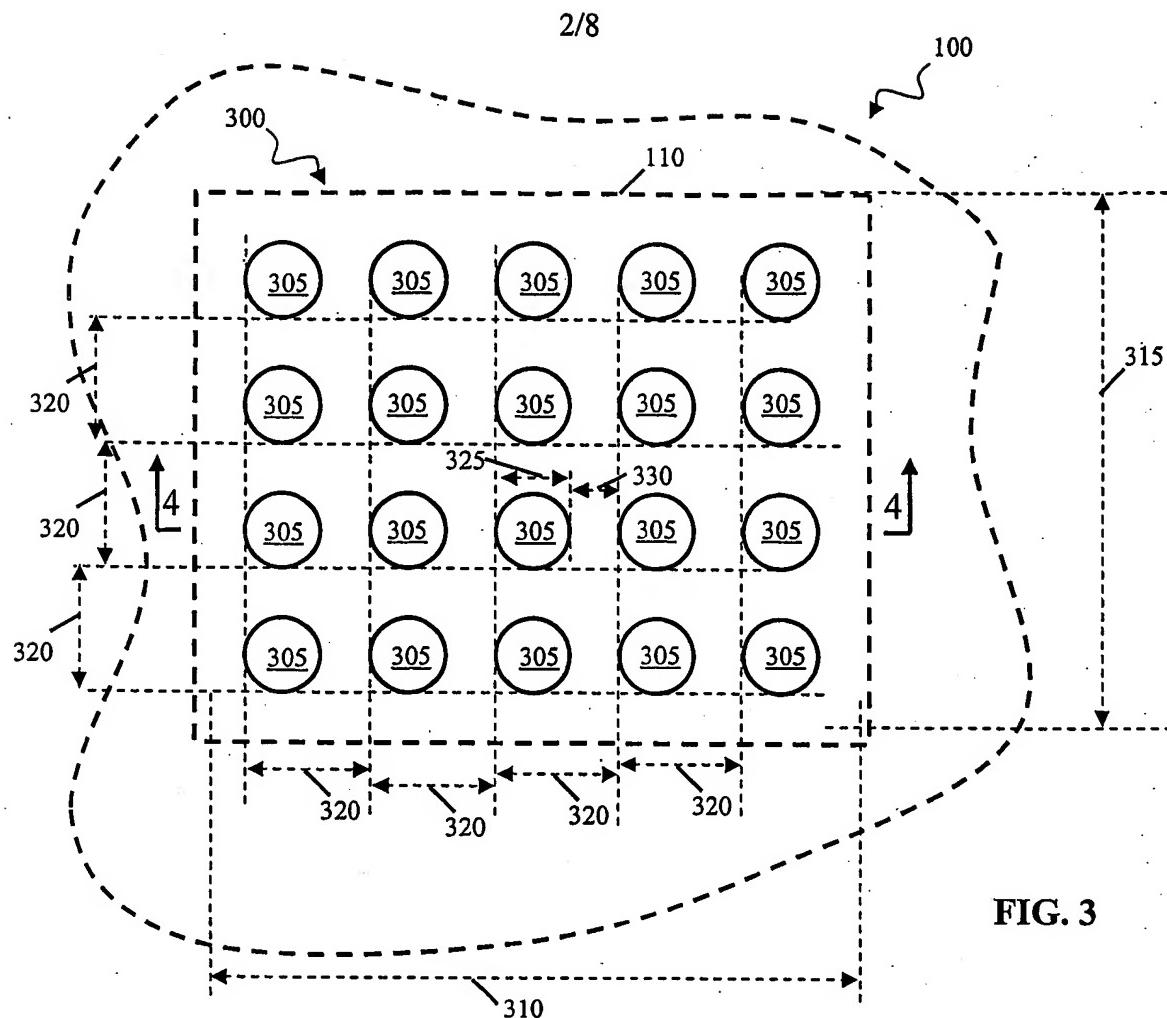


FIG. 3

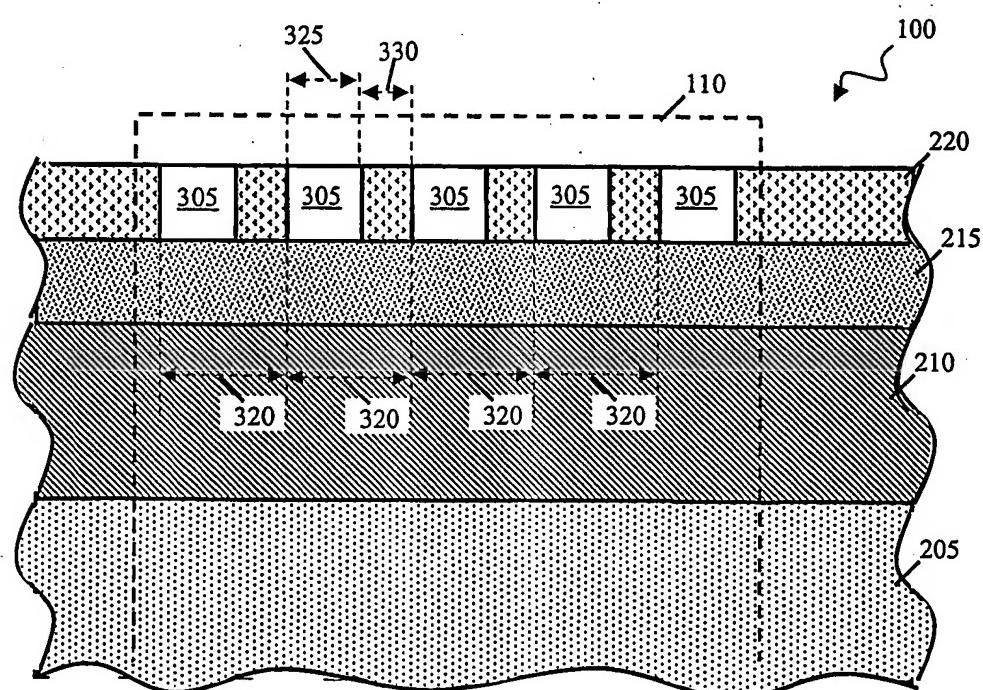


FIG. 4

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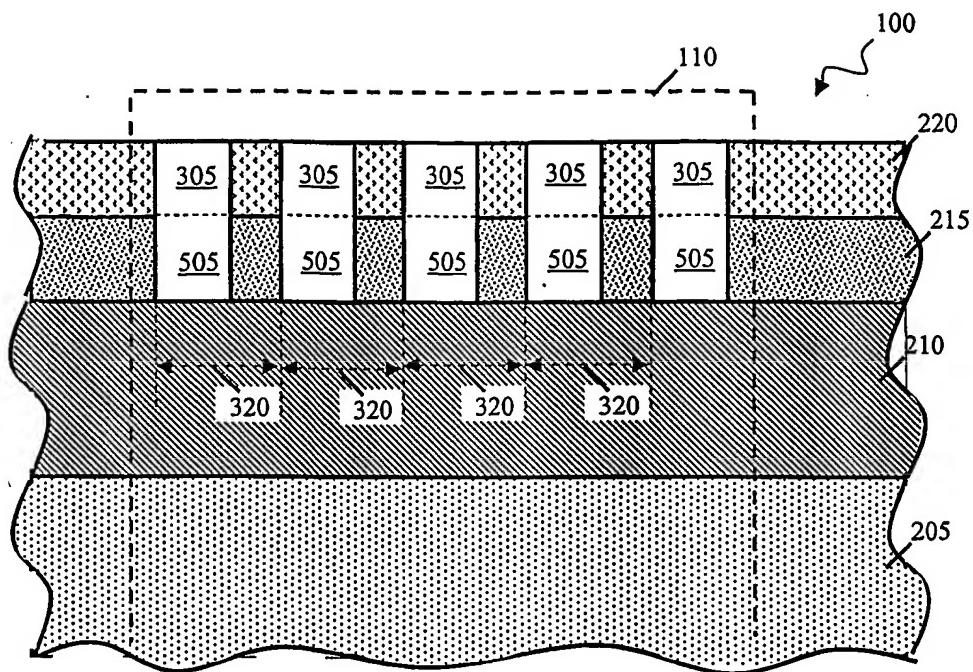


FIG. 5

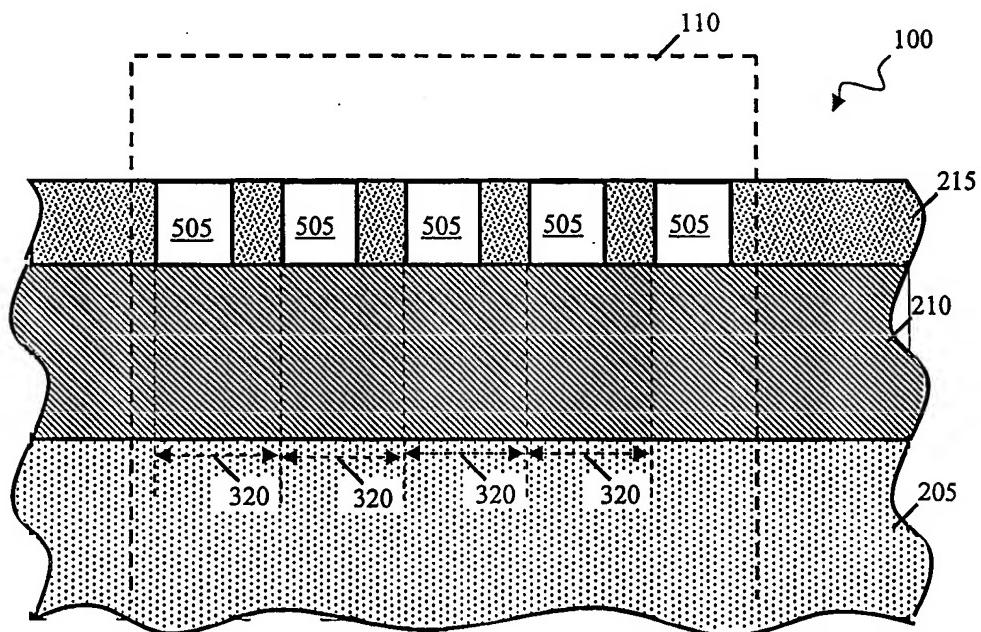


FIG. 6

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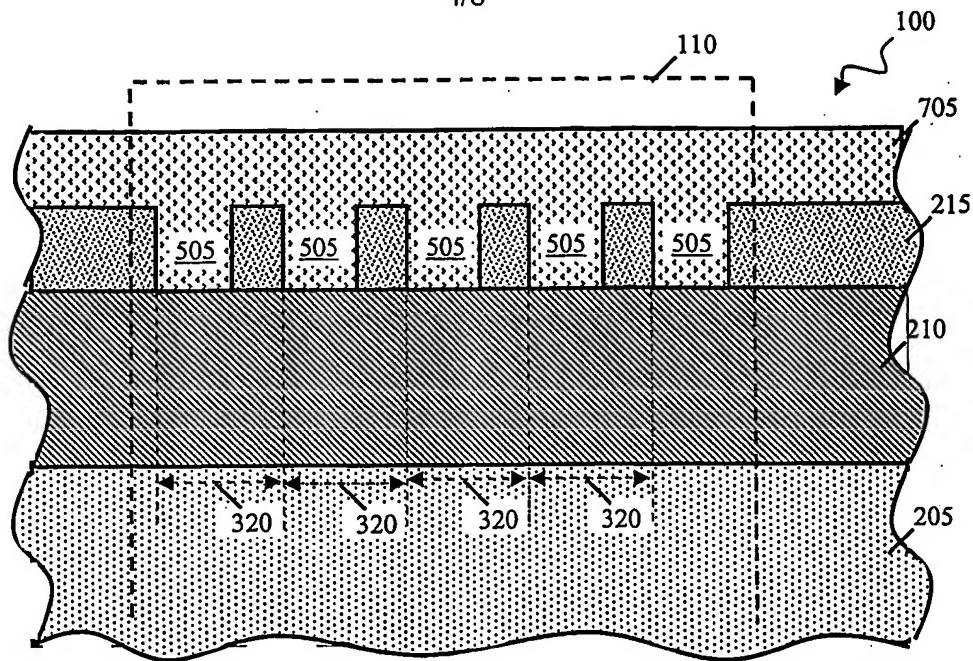


FIG. 7

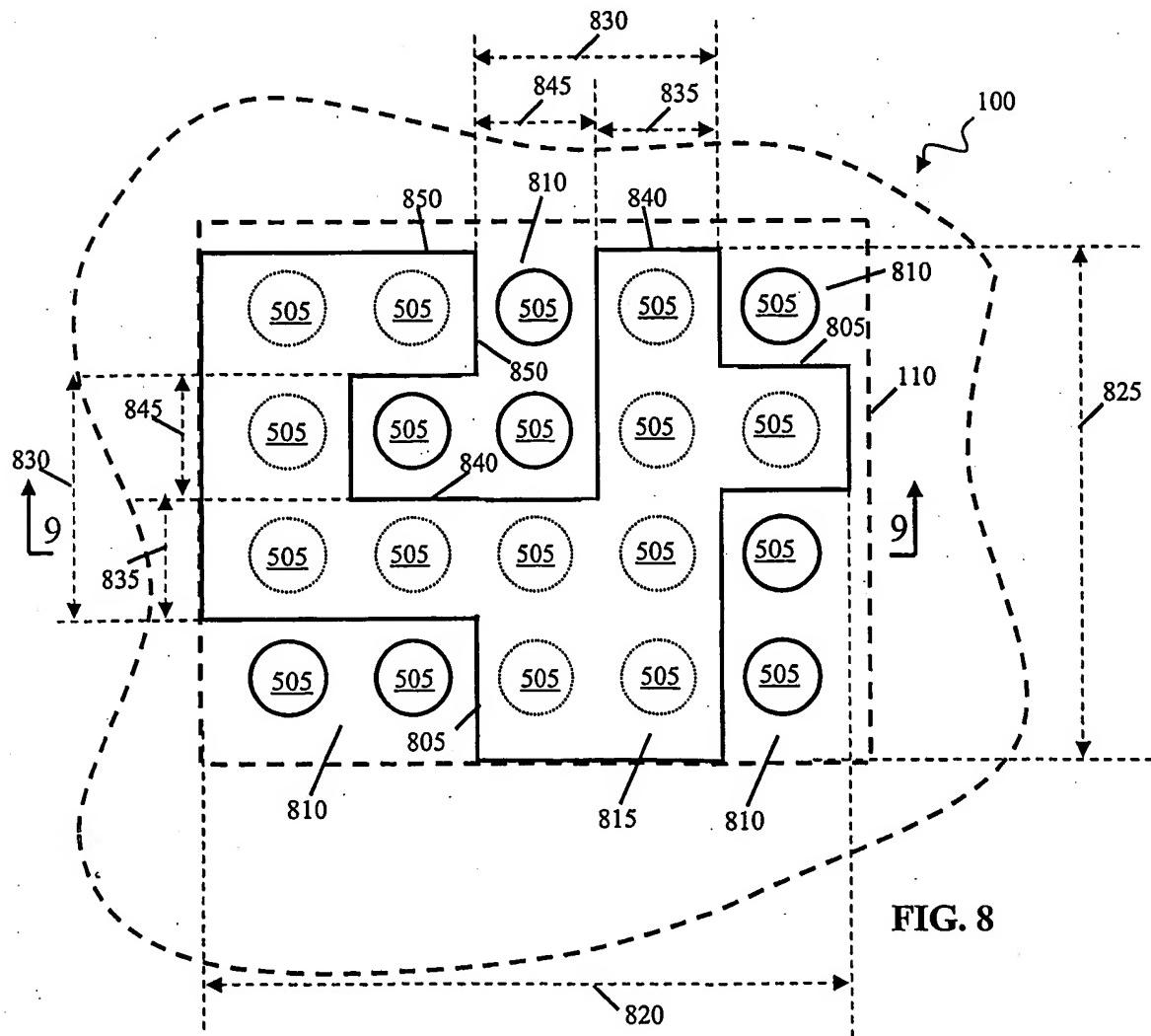


FIG. 8

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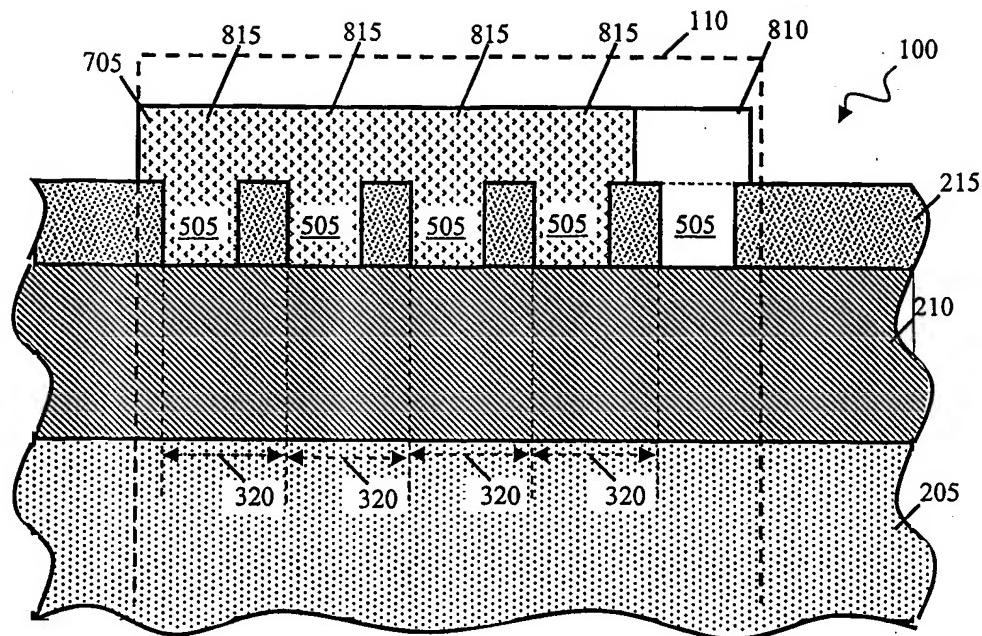


FIG. 9

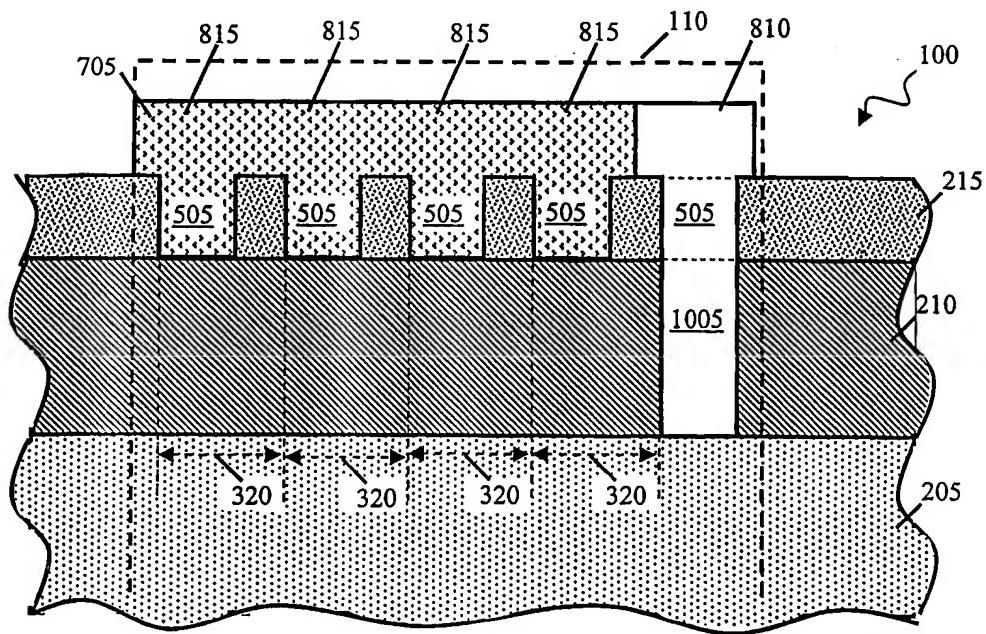
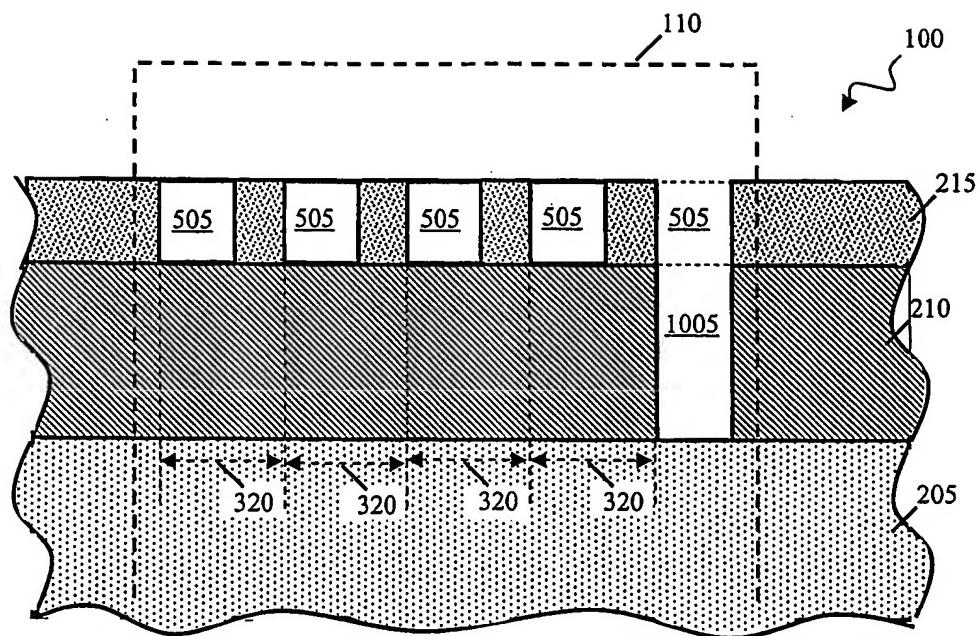


FIG. 10

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**FIG. 11**

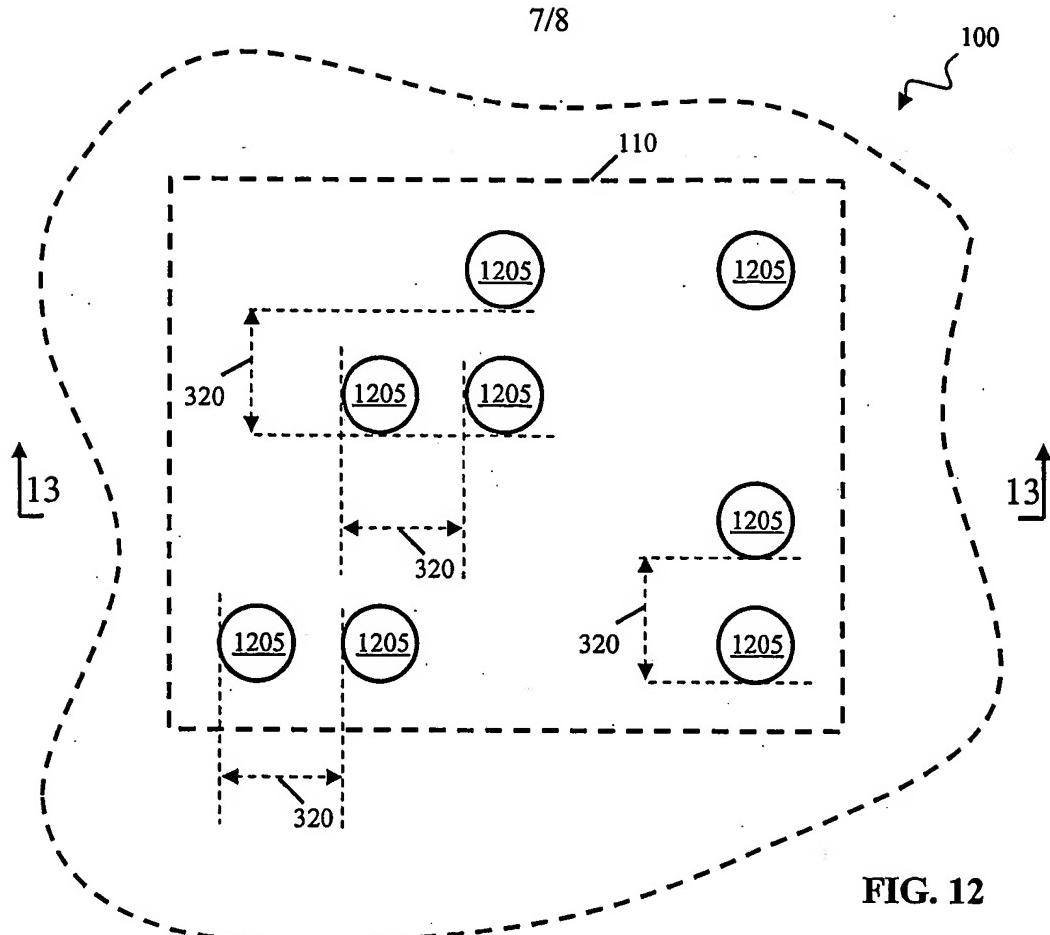


FIG. 12

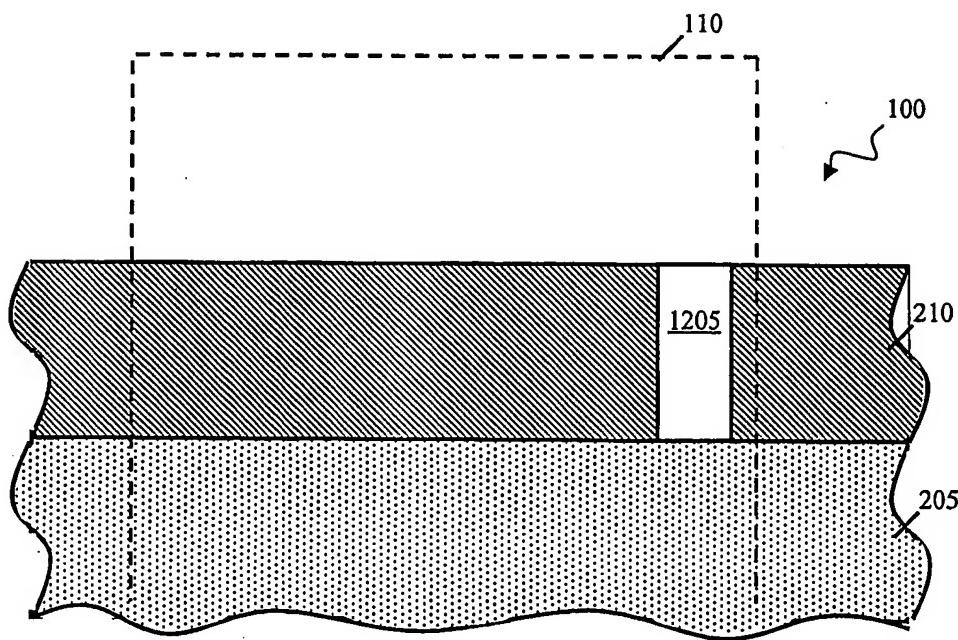


FIG. 13

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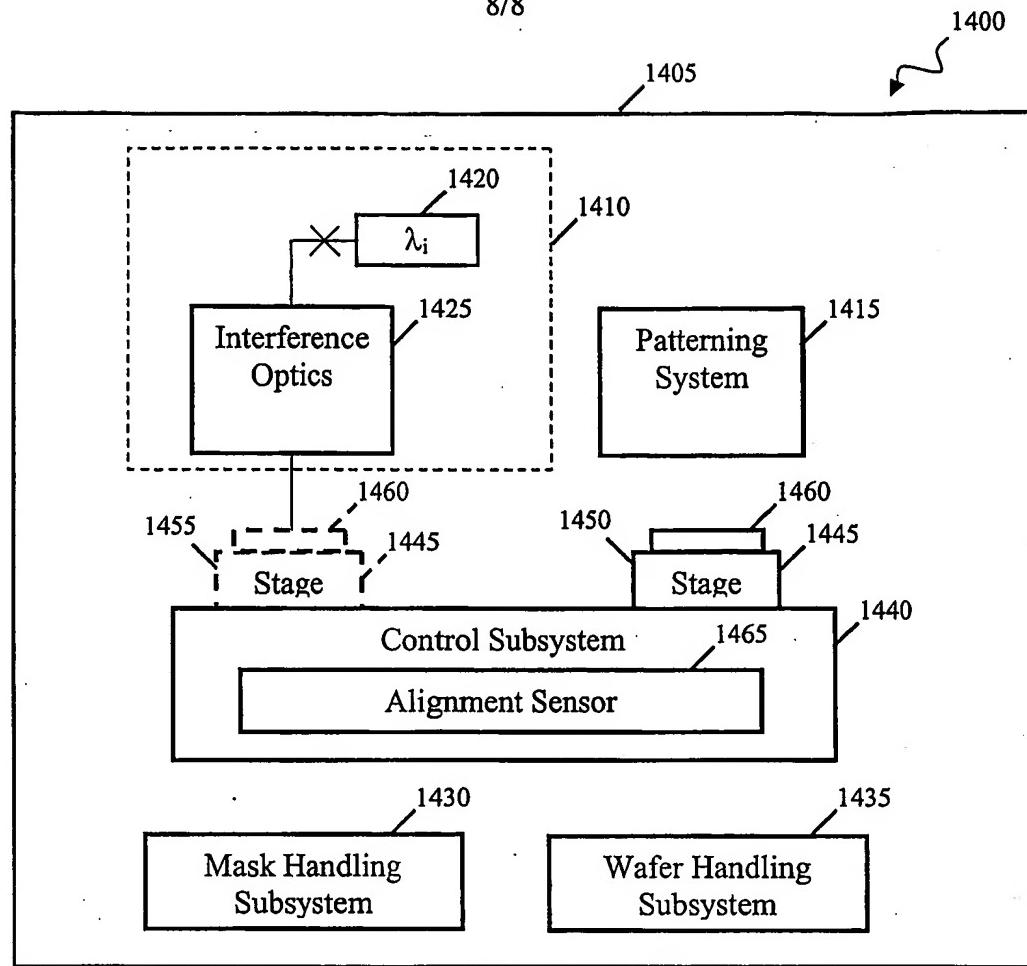


FIG. 14

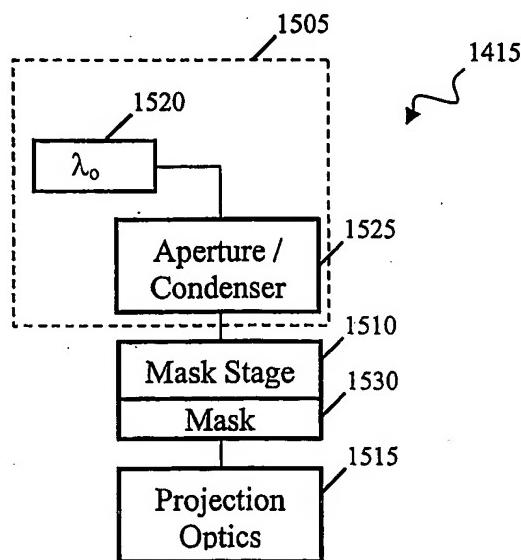


FIG. 15

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(54) Title: MULTISTEP PROCESS FOR CREATING IRREGULARITIES IN A REPEATING ARRAY OF PATTERN ELEMENTS

(57) Abstract: Systems and techniques for printing substrates. In one implementation, a method includes patterning a substrate with a substantially arbitrary arrangement of features by introducing irregularity into a repeating array of features.

INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
 IPC 7 G03F7/00 G03F7/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 517 280 A (OKAMOTO ET AL) 14 May 1985 (1985-05-14) Y the whole document -----	1-5, 8-13, 18-32 6,7, 14-17
X	US 5 415 835 A (BRUECK ET AL) 16 May 1995 (1995-05-16) the whole document -----	1-32
X	WO 97/48021 A (HOLOGRAPHIC LITHOGRAPHY SYSTEMS; HOBBS, DOUGLAS, S) 18 December 1997 (1997-12-18) the whole document -----	1-5, 8-13, 18-32
Y	US 5 759 744 A (BRUECK ET AL) 2 June 1998 (1998-06-02) the whole document -----	6,7, 14-17
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Date of the actual completion of the International search

14 October 2005

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Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P, X	US 2004/110092 A1 (LIN CHIN-HSIANG) 10 June 2004 (2004-06-10) the whole document -----	1-32
A	WO 03/071587 A (UNIVERSITY OF DELAWARE; PRATHER, DENNIS, W; MURAKOWSKI, JANUSZ) 28 August 2003 (2003-08-28) -----	

INTERNATIONAL SEARCH REPORT

/US2004/033434

Patent document cited in search report		Publication date		Patent family member(s)		Publication date
US 4517280	A	14-05-1985	DE EP	3370078 D1 0110184 A1		09-04-1987 13-06-1984
US 5415835	A	16-05-1995		NONE		
WO 9748021	A	18-12-1997	AU EP JP KR	3222397 A 0907905 A1 2002501669 T 2000016497 A		07-01-1998 14-04-1999 15-01-2002 25-03-2000
US 5759744	A	02-06-1998		NONE		
US 2004110092	A1	10-06-2004	US	2005147921 A1		07-07-2005
WO 03071587	A	28-08-2003	AU	2003217542 A1		09-09-2003

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